CLAIMS:

1. 1. System comprising

- a first processor bus (10; 70; 90),
- a first processor (P1) being connectable to the first processor bus (10; 70; 90),
- a first direct memory access unit (45; 83; 101) with a first external direct memory access channel (47; 85; 106), the first direct memory access unit (45; 83; 101) being connectable to the first processor bus (10; 70; 90),
- a first programmable unit (34; 82; 92) being connectable via the first external direct memory access channel (47; 85; 106) to the first direct memory access unit (45; 83; 101), said first programmable unit (34; 82; 92) being programmable by the first processor (P1),
- a first shareable unit (13; 76; 93) being connectable to the first processor bus (10; 70; 90),
- a second processor bus (20; 80; 100),
- a second processor (P2) being connectable to the second processor bus (20; 80; 100),
- a second direct memory access unit (35; 73; 93) with a second external direct memory access channel (36; 75; 96), the second direct memory access unit (35; 73; 93) being connectable to the second processor bus (20; 80; 100),
- a second programmable unit (44; 72; 92) being connectable via the second external direct memory access channel (36; 75; 95) to the second direct memory access unit (35; 73; 93), said second programmable unit (44; 72; 92) being programmable by the second processor (P2), and
- a second shareable unit (23; 86; 103) being connected to the processor bus (20; 80; 100),

wherein a first bi-directional communication channel is establishable between the first shareable unit (13; 76; 93) and the second processor (P2), and a second bi-directional communication channel is establishable between the second shareable unit (23; 86; 103) and the first processor (P1).

2. The system of claim 1, wherein the first bi-directional communication channel and/or the second bi-directional communication channel are half-duplex channels or full-duplex channels.

3. The system of claim 1, wherein the processor (P1) and the processor (P2) are similar from an architectural point of view.

4. The system of claim 1, wherein the processor (P1) and the processor (P2) are implementations of the same type of processor design.

5. The system of claim 1, wherein the processor (P1) and the processor (P2) are implementations of different types of processor design.

6. The system of the claims 1 - 5, wherein the shareable unit (13; 76; 93; 23; 86; 103) is either of the following: a memory, a peripheral, an interface, an input device, an output device.

7. The system of the claims 1 - 5, wherein one of the two integrated processors (P1, P2) is a central processing unit (CPU), a microprocessor, a digital signal processor (DSP), a system controller (SC), a co-processor, or an auxiliary processor.

8. The system of the claims 1 - 5, wherein the first programmable unit (34; 82; 92) and/or the second programmable unit (44; 72; 92) comprises a processor interface (50; 60; 110; 120), a direct access unit core (52; 62; 112; 122), and two external direct memory access channel interfaces (51; 53; 61; 63; 111; 113; 121; 123).

9. The system of claim 8, wherein the processor interface (50; 60; 110; 120) has a programming link (12, 22; 32, 42; 51, 52; 74, 84; 94, 104) either for connecting to a processor bus (10, 20; 70, 80; 90, 100) or for connecting to a processor (P1, P2).

10. The system of any of the preceding claims, wherein the communication channels are establishable for transferring data and/or control information to and from the shareable unit (13; 76; 93; 23; 86; 103).

11. A computing device comprising a first processor (P1) and a second processor (P2) being arranged on a common semiconductor die and being operably connected via bi-directional communication channels for exchanging information, the computing device further comprising

- a first processor bus (10; 70; 90), the first processor (P1) being connectable to the first processor bus (10; 70; 90),
- a first direct memory access unit (45; 83; 101) with a first external direct memory access channel (47; 85; 106), the first direct memory access unit (45; 83; 101) being connectable to the first processor bus (10; 70; 90),
- a first programmable unit (34; 82; 92) being connectable via the first external direct memory access channel (47; 85; 106) to the first direct memory access unit (45; 83; 101), said first programmable unit (34; 82; 92) being programmable by the first processor (P1),
- a first shareable unit (13; 76; 93) being connectable to the first processor bus (10; 70; 90),
- a second processor bus (20; 80; 100), the second processor (P2) being connectable to the second processor bus (20; 80; 100),
- a second direct memory access unit (35; 73; 93) with a second external direct memory access channel (36; 75; 96), the second direct memory access unit (35; 73; 93) being connectable to the second processor bus (20; 80; 100),
- a second programmable unit (44; 72; 92) being connectable via the second external direct memory access channel (36; 75; 96) to the second direct memory access unit (35; 73; 93), said second programmable unit (44; 72; 92) being programmable by the second processor (P2), and
- a second shareable unit (23; 86; 103) being connected to the processor bus (20; 80; 100).

12. The computing device of claim 11 being part of a PDA, a handheld computer, a palm top computer, a cellular phone, or a cordless phone.